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1 **Gate-level aged timing simulation methodology for hot-carrier reliab assurance**
Kawakami, Y.; Jingkun Fang; Yonezawa, H.; Iwanishi, N.; Lifeng Wu; I-Hsien A.; Koike, N.; Ping Chen; Chune-Sin Yeh; Zhihong Liu;
Design Automation Conference, 2000. Proceedings of the ASP-DAC 2000. Asia South Pacific , 25-28 Jan. 2000
Pages:289 - 294

[Abstract] [PDF Full-Text (408 KB)] **IEEE CNF**

2 **Ratio based hot-carrier degradation modeling for aged timing simul of millions of transistors digital circuits**
Yonezawa, H.; Jingjun Fang; Kawakami, Y.; Iwanishi, N.; Lifeng Wu; Chen, A Koike, N.; Ping Chen; Chune-Sin Yeh; Zhihong Liu;
Electron Devices Meeting, 1998. IEDM '98 Technical Digest., International , 6-Dec. 1998
Pages:93 - 96

[Abstract] [PDF Full-Text (280 KB)] **IEEE CNF**

3 **The application of wavelet transform to the study of time prediction errors in clocks for use in CDMA digital communication systems**
Ujiie, H.; Maruo, K.; Watanabe, P.; Goka, S.; Sekimoto, H.;
European Frequency and Time Forum, 1999 and the IEEE International Frequ Control Symposium, 1999., Proceedings of the 1999 Joint Meeting of the , Vo 1 , 13-16 April 1999
Pages:182 - 185 vol.1

[Abstract] [PDF Full-Text (300 KB)] **IEEE CNF**

4 **An economic model to estimate software rewriting and replacement times**
Taizan Chan; Siu Leung Chung; Teck Hua Ho;

Software Engineering, IEEE Transactions on , Volume: 22 , Issue: 8 , Aug. 19
Pages:580 - 598

[Abstract] [PDF Full-Text (1808 KB)] **IEEE JNL**

5 **Digital automatic gain control for hearing aids**
Camilleri, P.F.; Sobelman, G.E.;
VLSI Signal Processing, VII, 1994., [Workshop on] , 26-28 Oct. 1994
Pages:3 - 12

[Abstract] [PDF Full-Text (340 KB)] **IEEE CNF**

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Kawakami, Y.; Jingkun Fang; Yonezawa, H.; Iwanishi, N.; Lifeng Wu; I-Hsien A.; Koike, N.; Ping Chen; Chune-Sin Yeh; Zhihong Liu;

Design Automation Conference, 2000. Proceedings of the ASP-DAC 2000. Asia South Pacific , 25-28 Jan. 2000
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1 Gate-level aged timing simulation methodology for hot-carrier reliability assurance

Yoshiyuki Kawakami, Jingkun Fang, Hirokazu Yonezawa, Nobufusa Iwanishi, Lifeng Wu, Alvin I-Hsien Chen, Norio Koike, Ping Chen, Chune-Sin Yeh, Zhihong Liu

January 2000 **Proceedings of the 2000 conference on Asia South Pacific design automation**

Full text available: pdf(432.93 KB) Additional Information: full citation, references

2 Layout-driven hot-carrier degradation minimization using logic restructuring techniques

Chih-Wei Chang, Kai Wang, Malgorzata Marek-Sadowska

June 2001 **Proceedings of the 38th conference on Design automation**

Full text available: pdf(152.85 KB) Additional Information: full citation, references, index terms

3 Computer simulation of U.S. Army officer professional development

Michael L. McGinnis, James L. Kays, Pamela Slaten

December 1994 **Proceedings of the 26th conference on Winter simulation**

Full text available: pdf(822.42 KB) Additional Information: full citation, references, citings, index terms

4 A LOTOS extension for the performance analysis of distributed systems

Marco Ajmone Marsan, Andrea Bianco, Luigi Ciminiera, Riccardo Sisto, Adriano Valenzano

April 1994 **IEEE/ACM Transactions on Networking (TON)**, Volume 2 Issue 2

Full text available: pdf(1.59 MB) Additional Information: full citation, references, citings, index terms

5 A Five-Phase Reservation Protocol (FPRP) for Mobile Ad Hoc Networks

Chenxi Zhu, M. S. Corson

September 2001 **Wireless Networks**, Volume 7 Issue 4

Full text available: pdf(211.39 KB) Additional Information: full citation, abstract, references, index terms

A new single channel, time division multiple access (TDMA)-based broadcast scheduling protocol, termed the Five-Phase Reservation Protocol (FPRP), is presented for mobile ad hoc networks. The protocol jointly and simultaneously performs the tasks of channel access and node broadcast scheduling. The protocol allows nodes to make reservations within TDMA broadcast schedules. It employs a contention-based mechanism with which nodes compete

with each other to acquire TDMA slots. The FPRP is free of ...

Keywords: ad hoc networks, broadcast slot assignment, graph coloring, slotted-Aloha, time-division-multiple-access

6 Cache Memories
Alan Jay Smith
September 1982 **ACM Computing Surveys (CSUR)**, Volume 14 Issue 3
Full text available: pdf(4.61 MB) Additional Information: full citation, references, citings, index terms

7 Reliability Issues in Computing System Design
B. Randell, P. Lee, P. C. Treleaven
June 1978 **ACM Computing Surveys (CSUR)**, Volume 10 Issue 2
Full text available: pdf(3.95 MB) Additional Information: full citation, references, citings, index terms

8 Information and control in gray-box systems
Andrea C. Arpaci-Dusseau, Remzi H. Arpaci-Dusseau
October 2001 **ACM SIGOPS Operating Systems Review , Proceedings of the eighteenth ACM symposium on Operating systems principles**, Volume 35 Issue 5
Full text available: pdf(1.59 MB) Additional Information: full citation, abstract, references, citings, index terms

In modern systems, developers are often unable to modify the underlying operating system. To build services in such an environment, we advocate the use of *gray-box* techniques. When treating the operating system as a gray-box, one recognizes that not changing the OS restricts, but does not completely obviate, both the *information* one can acquire about the internal state of the OS and the *control* one can impose on the OS. In this paper, we develop and investigate three gray-bo ...

9 File system aging—increasing the relevance of file system benchmarks
Keith A. Smith, Margo I. Seltzer
June 1997 **ACM SIGMETRICS Performance Evaluation Review , Proceedings of the 1997 ACM SIGMETRICS international conference on Measurement and modeling of computer systems**, Volume 25 Issue 1
Full text available: pdf(1.81 MB) Additional Information: full citation, abstract, references, citings, index terms

Benchmarks are important because they provide a means for users and researchers to characterize how their workloads will perform on different systems and different system architectures. The field of file system design is no different from other areas of research in this regard, and a variety of file system benchmarks are in use, representing a wide range of the different user workloads that may be run on a file system. A realistic benchmark, however, is only one of the tools that is required in ...

10 Experimental comparison of memory management policies for NUMA multiprocessors
Richard P. Larowe, Carla Schlatter Ellis
November 1991 **ACM Transactions on Computer Systems (TOCS)**, Volume 9 Issue 4
Full text available: pdf(3.17 MB) Additional Information: full citation, references, citings, index terms

11 Parallelization of radiance for real time interactive lighting visualization walkthroughs
David Robertson, Kevin Campbell, Stephen Lau, Terry Ligocki
January 1999 **Proceedings of the 1999 ACM/IEEE conference on Supercomputing**

(CDROM)

Full text available: pdf(207.14 KB) Additional Information: full citation, references, index terms

Keywords: computer graphics, lighting visualization, parallelization, radiance, supercomputers, visualization

12 Mining a stream of transactions for customer patterns

Diane Lambert, José C. Pinheiro

August 2001 **Proceedings of the seventh ACM SIGKDD international conference on Knowledge discovery and data mining**

Full text available: pdf(532.89 KB) Additional Information: full citation, abstract, references, citings, index terms

Transaction data can arrive at a ferocious rate in the order that transactions are completed. The data contain an enormous amount of information about *customers*, not just transactions, but extracting up-to-date customer information from an ever changing stream of data and mining it in real-time is a challenge. This paper describes a statistically principled approach to designing short, accurate summaries or *signatures* of high dimensional customer behavior that can be kept current w ...

Keywords: Approximate queries, customer profiles, dynamic database, histograms, incremental updates, massive data, signatures

13 Interactive global illumination in dynamic scenes

Parag Tole, Fabio Pellacini, Bruce Walter, Donald P. Greenberg

July 2002 **ACM Transactions on Graphics (TOG) , Proceedings of the 29th annual conference on Computer graphics and interactive techniques**, Volume 21 Issue 3

Full text available: pdf(13.82 MB) Additional Information: full citation, abstract, references, citings, index terms

In this paper, we present a system for interactive computation of global illumination in dynamic scenes. Our system uses a novel scheme for caching the results of a high quality pixel-based renderer such as a bidirectional path tracer. The Shading Cache is an object-space hierarchical subdivision mesh with lazily computed shading values at its vertices. A high frame rate display is generated from the Shading Cache using hardware-based interpolation and texture mapping. An image space sampling sc ...

Keywords: Monte Carlo techniques, illumination, parallel computing, ray tracing, rendering, rendering systems

14 Join processing in database systems with large main memories

Leonard D. Shapiro

August 1986 **ACM Transactions on Database Systems (TODS)**, Volume 11 Issue 3

Full text available: pdf(1.41 MB) Additional Information: full citation, abstract, references, citings, index terms, review

We study algorithms for computing the equijoin of two relations in a system with a standard architecture hut with large amounts of main memory. Our algorithms are especially efficient when the main memory available is a significant fraction of the size of one of the relations to he joined; but they can be applied whenever there is memory equal to approximately the square root of the size of one relation. We present a new algorithm which is a hybrid of two hash-based algorithms and which dom ...

15 Real-time protocol analysis for detecting link-state routing protocol attacks

Ho-Yen Chang, S. Felix Wu, Y. Frank Jou

February 2001 **ACM Transactions on Information and System Security (TISSEC)**, Volume 4 Issue 1

Full text available: pdf(252.10 KB) Additional Information: full citation, abstract, references, citings, index terms

A real-time knowledge-based network intrusion-detection model for a link-state routing protocol is presented for the OSPF protocol. This model includes three layers: a data process layer to parse packets and dispatch data; and event abstractor to abstract predefined real-time events for the link-state routing protocol; and an extended timed finite state machine to express the real-time behavior of the protocol engine and to ...

Keywords: OSPF attacks, event correlation, knowledge-based IDS, link-state routing protocol security, real-time misuse intrusion detection, real-time network protocol analysis, timed finite state machine

16 Hybrid static-dynamic communication scheduling for parallel systems

David R. Surma, Edwin H.-M. Sha

April 1997 **Proceedings of the 1997 ACM symposium on Applied computing**

Full text available: pdf(589.84 KB) Additional Information: full citation, references, index terms

Keywords: collision graph, communication, data-flow graph, hybrid scheduling

17 The interdisciplinary study of coordination

Thomas W. Malone, Kevin Crowston

March 1994 **ACM Computing Surveys (CSUR)**, Volume 26 Issue 1

Full text available: pdf(584.94 KB) Additional Information: full citation, abstract, references, citings, index terms, review

This survey characterizes an emerging research area, sometimes called coordination theory, that focuses on the interdisciplinary study of coordination. Research in this area uses and extends ideas about coordination from disciplines such as computer science, organization theory, operations research, economics, linguistics, and psychology. A key insight of the framework presented here is that coordination can be seen as the process of managing dependencies ...

Keywords: computer-supported cooperative work, coordination, coordination science, coordination theory, groupware

18 Continuous program optimization: A case study

Thomas Kistler, Michael Franz

July 2003 **ACM Transactions on Programming Languages and Systems (TOPLAS)**, Volume 25 Issue 4

Full text available: pdf(877.67 KB) Additional Information: full citation, abstract, references, index terms

Much of the software in everyday operation is not making optimal use of the hardware on which it actually runs. Among the reasons for this discrepancy are hardware/software mismatches, modularization overheads introduced by software engineering considerations, and the inability of systems to adapt to users' behaviors.A solution to these problems is to delay code generation until load time. This is the earliest point at which a piece of software can be fine-tuned to the actual capabilities of the ...

Keywords: Dynamic code generation, continuous program optimization, dynamic reoptimization

19

A new concept for accurate modeling of VLSI interconnections and its application for timing simulation

B. Wunder, G. Lehmann, K. Müller-Glaser

September 1996 **Proceedings of the conference on European design automation**

Full text available: pdf(415.21 KB) Additional Information: full citation, references, index terms

20 Scaling up: a research agenda for software engineering

CORPORATE Computer Science and Technology Board

March 1990 **Communications of the ACM**, Volume 33 Issue 3

Full text available: pdf(1.51 MB) Additional Information: full citation, abstract, references, citings, index terms, review

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PGPUB-DOCUMENT-NUMBER: 20020022949
PGPUB-FILING-TYPE: new
DOCUMENT-IDENTIFIER: US 20020022949 A1

TITLE: Apparatus and method for calculating temporal deterioration margin amount of LSI, and LSI inspection method

PUBLICATION-DATE: February 21, 2002

INVENTOR-INFORMATION:

NAME	CITY	STATE	COUNTRY	RULE-47
Yonezawa, Hirokazu	Hyogo		JP	
Kawakami, Yoshiyuki	Osaka		JP	
Iwanishi, Nobufusa	Osaka		JP	

US-CL-CURRENT: 703/14

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☐ 2. Document ID: US 5255086 A

L9: Entry 2 of 9 File: USPT Oct 19, 1993

US-PAT-NO: 5255086
DOCUMENT-IDENTIFIER: US 5255086 A

TITLE: Method and apparatus for RF data transfer in a CATV system

DATE-ISSUED: October 19, 1993

INVENTOR-INFORMATION:

NAME	CITY	STATE	ZIP CODE	COUNTRY
McMullan, Jr.; Jay C.	Doraville	GA		
Naddor; David J.	Doraville	GA		
Beyers, II; Robert J.	Snellville	GA		

US-CL-CURRENT: 725/131; 725/1, 725/104, 725/125

☐ 3. Document ID: US 5235619 A

L9: Entry 3 of 9 File: USPT Aug 10, 1993

US-PAT-NO: 5235619
DOCUMENT-IDENTIFIER: US 5235619 A

TITLE: Cable television radio frequency subscriber data transmission apparatus and RF return method

DATE-ISSUED: August 10, 1993

INVENTOR-INFORMATION:

NAME	CITY	STATE	ZIP CODE	COUNTRY
Beyers, II; Robert J.	Snellville	GA		
Bramhall; Charles R.	Norcross	GA		
Durden; Gregory S.	Jonesboro	GA		
Edwards; Robert J.	Lawrenceville	GA		
Haman, Jr.; Ray T.	Buluth	GA		
Hoder; Douglas J.	Lakewood	OH		
Huntley; Donald R.	Roswell	GA		
Kennedy; John A.	Doraville	GA		
McGinty, Jr.; Emory L.	Lilburn	GA		
McMullan, Jr.; Jay C.	Doraville	GA		
Naddor; David J.	Doraville	GA		
Schaubs; Randolph J.	Stone Mountain	GA		
Still; Jesse M.	Woodstock	GA		
Wasilewski; Anthony J.	Alpharetta	GA		
West, Jr.; Lamar E.	Maysville	GA		
White; Donovan S.	Alpharetta	GA		

US-CL-CURRENT: 375/260; 375/267, 725/114, 725/125, 725/131, 725/25, 725/37

Full | Title | Citation | Front | Review | Classification | Date | Reference | Claims | KWMC | Draw De

☐ 4. Document ID: US 5225902 A

L9: Entry 4 of 9 File: USPT Jul 6, 1993

US-PAT-NO: 5225902
DOCUMENT-IDENTIFIER: US 5225902 A

TITLE: Automatic frequency selection in a bi-directional cable television system

DATE-ISSUED: July 6, 1993

INVENTOR-INFORMATION:

NAME	CITY	STATE	ZIP CODE	COUNTRY
McMullan, Jr.; Jay C.	Doraville	GA		

US-CL-CURRENT: 725/121; 455/59, 455/62, 455/67.11, 725/1, 725/114

Full | Title | Citation | Front | Review | Classification | Date | Reference | Claims | KWMC | Draw De

☐ 5. Document ID: US 5155590 A

L9: Entry 5 of 9 File: USPT Oct 13, 1992

US-PAT-NO: 5155590
DOCUMENT-IDENTIFIER: US 5155590 A

TITLE: System for data channel level control

DATE-ISSUED: October 13, 1992

INVENTOR-INFORMATION:

NAME	CITY	STATE	ZIP CODE	COUNTRY
Beyers, II; Robert J.	Snellville	GA		
Bramhall; Charles R.	Norcross	GA		
Durden; Gregory S.	Jonesboro	GA		
Edwards; Robert J.	Lawrenceville	GA		
Haman, Jr.; Ray T.	Duluth	GA		
Hoder; Douglas J.	Lakewood	GA		
Huntley; Donald R.	Roswell	GA		
Kennedy; John A.	Doraville	GA		
McGinty, Jr.; Emory L.	Lilburn	GA		
McMullan, Jr.; Jay C.	Doraville	GA		
Naddor; David J.	Doraville	GA		
Schaubs; Randolph J.	Stone Mountain	GA		
Still; Jesse M.	Woodstock	GA		
Wasilewski; Anthony J.	Alpharetta	GA		
West, Jr.; Lamar E.	Maysville	GA		
White; Donovan S.	Alpharetta	GA		

US-CL-CURRENT: 725/107; 455/67.14, 455/71, 725/1, 725/104, 725/121

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☐ 6. Document ID: US 5142690 A

L9: Entry 6 of 9 File: USPT Aug 25, 1992

US-PAT-NO: 5142690
DOCUMENT-IDENTIFIER: US 5142690 A

TITLE: Cable television radio frequency data processor

DATE-ISSUED: August 25, 1992

INVENTOR-INFORMATION:

NAME	CITY	STATE	ZIP CODE	COUNTRY
McMullan, Jr.; Jay C.	Doraville	GA		

Hoder; Douglas J.	Lakewood	OH
Huntley; Donald R.	Roswell	GA

US-CL-CURRENT: 725/124; 370/249, 455/134, 455/67.11, 725/1, 725/104, 725/121

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☐ 7. Document ID: US 5132786 A

L9: Entry 7 of 9 File: USPT Jul 21, 1992

US-PAT-NO: 5132786
DOCUMENT-IDENTIFIER: US 5132786 A
**** See image for Certificate of Correction ****

TITLE: Color converting system for image processing equipment

DATE-ISSUED: July 21, 1992

INVENTOR-INFORMATION:

NAME	CITY	STATE	ZIP CODE	COUNTRY
Ishiwata; Masahiro	Ebina			JP

US-CL-CURRENT: 358/500

Full | Title | Citation | Front | Review | Classification | Date | Reference | Claims | KWMC | Draw De

☐ 8. Document ID: US 5113251 A

L9: Entry 8 of 9 File: USPT May 12, 1992

US-PAT-NO: 5113251
DOCUMENT-IDENTIFIER: US 5113251 A
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TITLE: Editing control system and area editing system for image processing equipment

DATE-ISSUED: May 12, 1992

INVENTOR-INFORMATION:

NAME	CITY	STATE	ZIP CODE	COUNTRY
Ichiyanagi; Yoshio	Kanagawa			JP
Aoyama; Teruyuki	Kanagawa			JP

US-CL-CURRENT: 358/500; 358/453

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L9: Entry 9 of 9 File: USPT Mar 31, 1992

US-PAT-NO: 5101283
DOCUMENT-IDENTIFIER: US 5101283 A
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TITLE: Halftone image generating apparatus

DATE-ISSUED: March 31, 1992

INVENTOR-INFORMATION:

NAME	CITY	STATE	ZIP CODE	COUNTRY
Seki; Masao	Ebina			JP
Sasuga; Kazuyasu	Ebina			JP
Inoue; Yukiharu	Ebina			JP
Toyoda; Shinjiro	Ebina			JP

US-CL-CURRENT: 358/3.13; 358/3.03

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DOCUMENT-IDENTIFIER: US 20020022949 A1

TITLE: Apparatus and method for calculating temporal deterioration margin amount of LSI, and LSI inspection method

PUBLICATION-DATE: February 21, 2002

INVENTOR-INFORMATION:

NAME	CITY	STATE	COUNTRY	RULE-47
Yonezawa, Hirokazu	Hyogo		JP	
Kawakami, Yoshiyuki	Osaka		JP	
Iwanishi, Nobufusa	Osaka		JP	

US-CL-CURRENT: 703/14

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PGPUB-DOCUMENT-NUMBER: 20030055621
PGPUB-FILING-TYPE: new
DOCUMENT-IDENTIFIER: US 20030055621 A1

TITLE: Hot carrier circuit reliability simulation

PUBLICATION-DATE: March 20, 2003

INVENTOR-INFORMATION:

NAME	CITY	STATE	COUNTRY	RULE-47
Wu, Lifeng	Fremont	CA	US	
Liu, Zhihong	Cupertino	CA	US	
Chen, Alvin I.	San Jose	CA	US	
Choi, Jeong Y.	Portland	OR	US	
McGaughy, Bruce W.	Fremont	CA	US	

US-CL-CURRENT: 703/14

Full | Title | Citation | Front | Review | Classification | Date | Reference | Sequences | Attachments | Claims | KWIC | Draw De

☐ 2. Document ID: US 20020022949 A1

L6: Entry 2 of 7 File: PGPB Feb 21, 2002

PGPUB-DOCUMENT-NUMBER: 20020022949
PGPUB-FILING-TYPE: new
DOCUMENT-IDENTIFIER: US 20020022949 A1

TITLE: Apparatus and method for calculating temporal deterioration margin amount of LSI, and LSI inspection method

PUBLICATION-DATE: February 21, 2002

INVENTOR-INFORMATION:

NAME	CITY	STATE	COUNTRY	RULE-47
Yonezawa, Hirokazu	Hyogo		JP	
Kawakami, Yoshiyuki	Osaka		JP	
Iwanishi, Nobufusa	Osaka		JP	

US-CL-CURRENT: 703/14

Full | Title | Citation | Front | Review | Classification | Date | Reference | Sequences | Attachments | Claims | KWIC | Draw De

☐ 3. Document ID: US 20010032329 A1

L6: Entry 3 of 7 File: PGPB Oct 18, 2001

PGPUB-DOCUMENT-NUMBER: 20010032329
PGPUB-FILING-TYPE: new
DOCUMENT-IDENTIFIER: US 20010032329 A1

TITLE: Storage media being readable by a computer, and a method for designing a semiconductor integrated circuit device

PUBLICATION-DATE: October 18, 2001

INVENTOR-INFORMATION:

NAME	CITY	STATE	COUNTRY	RULE-47
Lee, Peter Maurice	Musashino		JP	
Yokomizo, Goichi	Nishitama		JP	

US-CL-CURRENT: 716/6; 716/5

Full | Title | Citation | Front | Review | Classification | Date | Reference | Sequences | Attachments | Claims | KWIC | Draw De

☐ 4. Document ID: US 20010029600 A1

L6: Entry 4 of 7 File: PGPB Oct 11, 2001

PGPUB-DOCUMENT-NUMBER: 20010029600
PGPUB-FILING-TYPE: new
DOCUMENT-IDENTIFIER: US 20010029600 A1

TITLE: Storage media being readable by a computer, and a method for designing a semiconductor integrated circuit device

PUBLICATION-DATE: October 11, 2001

INVENTOR-INFORMATION:

NAME	CITY	STATE	COUNTRY	RULE-47
Lee, Peter Maurice	Musashino		JP	
Yokomizo, Goichi	Nishitama		JP	

US-CL-CURRENT: 716/17

Full | Title | Citation | Front | Review | Classification | Date | Reference | Sequences | Attachments | Claims | KWIC | Draw De

☐ 5. Document ID: US 6634015 B2

L6: Entry 5 of 7 File: USPT Oct 14, 2003

US-PAT-NO: 6634015

DOCUMENT-IDENTIFIER: US 6634015 B2

TITLE: Computer-readable storage media stored with a delay library for designing a semiconductor integrated circuit device

DATE-ISSUED: October 14, 2003

INVENTOR-INFORMATION:

NAME	CITY	STATE	ZIP CODE	COUNTRY
Lee; Peter Maurice	Musashino			JP
Yokomizo; Goichi	Nishitama			JP

US-CL-CURRENT: 716/6; 438/14, 716/2, 716/4

Full | Title | Citation | Front | Review | Classification | Date | Reference | Claims | KWMC | Draw De

☐ 6. Document ID: US 6278964 B1

L6: Entry 6 of 7 File: USPT Aug 21, 2001

US-PAT-NO: 6278964
DOCUMENT-IDENTIFIER: US 6278964 B1

TITLE: Hot carrier effect simulation for integrated circuits

DATE-ISSUED: August 21, 2001

INVENTOR-INFORMATION:

NAME	CITY	STATE	ZIP CODE	COUNTRY
Fang; Jingkun	Santa Clara	CA		
Yonezawa; Hirokazu	Hyogo			JP
Wu; Lifeng	Fremont	CA		
Kawakami; Yoshiyuki	Osaka			JP
Iwanishi; Nobufusa	Osaka			JP
Chen; Alvin I-Hsien	Santa Clara	CA		
Koike; Norio	Kyoto			JP
Chen; Ping	Santa Clara	CA		
Yeh; Chune-Sin	Santa Clara	CA		
Liu; Zhihong	Sunnyvale	CA		

US-CL-CURRENT: 703/19; 703/14, 714/25, 714/47

Full | Title | Citation | Front | Review | Classification | Date | Reference | Claims | KWMC | Draw De

☐ 7. Document ID: US 5974247 A

L6: Entry 7 of 7 File: USPT Oct 26, 1999

US-PAT-NO: 5974247
DOCUMENT-IDENTIFIER: US 5974247 A

TITLE: Apparatus and method of LSI timing degradation simulation

DATE-ISSUED: October 26, 1999

INVENTOR-INFORMATION:

NAME	CITY	STATE	ZIP CODE	COUNTRY
Yonezawa; Hirokazu	Hyogo			JP

US-CL-CURRENT: 703/19; 703/20, 716/6

Full | Title | Citation | Front | Review | Classification | Date | Reference | Claims | KWMC | Draw De

Clear | Generate Collection | Print | Fwd Refs | Bkwd Refs | Generate OACS

Term	Documents
HOT	462431
HOTS	80
CARRIER	566347
CARRIERS	229652
(5 AND (HOT ADJ CARRIER)).PGPB,USPT.	7
(L5 AND HOT CARRIER).PGPB,USPT.	7

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Search Results - Record(s) 1 through 3 of 3 returned.

☐ 1. Document ID: US 20020022949 A1

Using default format because multiple data bases are involved.

L3: Entry 1 of 3 File: PGPB Feb 21, 2002

PGPUB-DOCUMENT-NUMBER: 20020022949
PGPUB-FILING-TYPE: new
DOCUMENT-IDENTIFIER: US 20020022949 A1

TITLE: Apparatus and method for calculating temporal deterioration margin amount of LSI, and LSI inspection method

PUBLICATION-DATE: February 21, 2002

INVENTOR-INFORMATION:

NAME	CITY	STATE	COUNTRY	RULE-47
Yonezawa, Hirokazu	Hyogo		JP	
Kawakami, Yoshiyuki	Osaka		JP	
Iwanishi, Nobufusa	Osaka		JP	

US-CL-CURRENT: 703/14

Full | Title | Citation | Front | Review | Classification | Date | Reference | Sequences | Attachments | Claims | KWIC | Draw De

☐ 2. Document ID: US 6278964 B1

L3: Entry 2 of 3 File: USPT Aug 21, 2001

US-PAT-NO: 6278964
DOCUMENT-IDENTIFIER: US 6278964 B1

TITLE: Hot carrier effect simulation for integrated circuits

DATE-ISSUED: August 21, 2001

INVENTOR-INFORMATION:

NAME	CITY	STATE	ZIP CODE	COUNTRY
Fang; Jingkun	Santa Clara	CA		
Yonezawa; Hirokazu	Hyogo			JP
Wu; Lifeng	Fremont	CA		
Kawakami; Yoshiyuki	Osaka			JP
Iwanishi; Nobufusa	Osaka			JP
Chen; Alvin I-Hsien	Santa Clara	CA		

Koike; Norio	Kyoto		JP
Chen; Ping	Santa Clara	CA	
Yeh; Chune-Sin	Santa Clara	CA	
Liu; Zhihong	Sunnyvale	CA	

US-CL-CURRENT: 703/19; 703/14, 714/25, 714/47

Full | Title | Citation | Front | Review | Classification | Date | Reference | Claims | KWMC | Draw De

☐ 3. Document ID: US 5974247 A

L3: Entry 3 of 3 File: USPT Oct 26, 1999

US-PAT-NO: 5974247
DOCUMENT-IDENTIFIER: US 5974247 A

TITLE: Apparatus and method of LSI timing degradation simulation

DATE-ISSUED: October 26, 1999

INVENTOR-INFORMATION:

NAME	CITY	STATE	ZIP CODE	COUNTRY
Yonezawa; Hirokazu	Hyogo			JP

US-CL-CURRENT: 703/19; 703/20, 716/6

Full | Title | Citation | Front | Review | Classification | Date | Reference | Claims | KWMC | Draw De

Clear | Generate Collection | Print | Fwd Refs | Bkwd Refs | Generate OACS

Term	Documents
AGED	41501
AGEDS	0
AGING	79637
AGINGS	62
(2 AND (AGED OR AGING)).PGPB,USPT.	3
(L2 AND (AGED OR AGING)).PGPB,USPT.	3

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Search Results - Record(s) 1 through 6 of 6 returned.

☐ 1. Document ID: US 20030054577 A1

Using default format because multiple data bases are involved.

L2: Entry 1 of 6 File: PGPB Mar 20, 2003

PGPUB-DOCUMENT-NUMBER: 20030054577
PGPUB-FILING-TYPE: new
DOCUMENT-IDENTIFIER: US 20030054577 A1

TITLE: Method for evaluating property of integrated circuit and method for designing the same

PUBLICATION-DATE: March 20, 2003

INVENTOR-INFORMATION:

NAME	CITY	STATE	COUNTRY	RULE-47
Yonezawa, Hirokazu	Hyogo		JP	
Ishikura, Satoshi	Osaka		JP	

US-CL-CURRENT: 438/14; 257/E21.525

Full | Title | Citation | Front | Review | Classification | Date | Reference | Sequences | Attachments | Claims | KWIC | Draw De

☐ 2. Document ID: US 20020022949 A1

L2: Entry 2 of 6 File: PGPB Feb 21, 2002

PGPUB-DOCUMENT-NUMBER: 20020022949
PGPUB-FILING-TYPE: new
DOCUMENT-IDENTIFIER: US 20020022949 A1

TITLE: Apparatus and method for calculating temporal deterioration margin amount of LSI, and LSI inspection method

PUBLICATION-DATE: February 21, 2002

INVENTOR-INFORMATION:

NAME	CITY	STATE	COUNTRY	RULE-47
Yonezawa, Hirokazu	Hyogo		JP	
Kawakami, Yoshiyuki	Osaka		JP	
Iwanishi, Nobufusa	Osaka		JP	

US-CL-CURRENT: 703/14

Full | Title | Citation | Front | Review | Classification | Date | Reference | Sequences | Attachments | Claims | KWMC | Draw De

☐ 3. Document ID: US 6278964 B1

L2: Entry 3 of 6 File: USPT Aug 21, 2001

US-PAT-NO: 6278964
DOCUMENT-IDENTIFIER: US 6278964 B1

TITLE: Hot carrier effect simulation for integrated circuits

DATE-ISSUED: August 21, 2001

INVENTOR-INFORMATION:

NAME	CITY	STATE	ZIP CODE	COUNTRY
Fang; Jingkun	Santa Clara	CA		
Yonezawa; Hirokazu	Hyogo			JP
Wu; Lifeng	Fremont	CA		
Kawakami; Yoshiyuki	Osaka			JP
Iwanishi; Nobufusa	Osaka			JP
Chen; Alvin I-Hsien	Santa Clara	CA		
Koike; Norio	Kyoto			JP
Chen; Ping	Santa Clara	CA		
Yeh; Chune-Sin	Santa Clara	CA		
Liu; Zhihong	Sunnyvale	CA		

US-CL-CURRENT: 703/19; 703/14, 714/25, 714/47

Full | Title | Citation | Front | Review | Classification | Date | Reference | Claims | KWMC | Draw De

☐ 4. Document ID: US 6104681 A

L2: Entry 4 of 6 File: USPT Aug 15, 2000

US-PAT-NO: 6104681
DOCUMENT-IDENTIFIER: US 6104681 A

TITLE: Disk apparatus

DATE-ISSUED: August 15, 2000

INVENTOR-INFORMATION:

NAME	CITY	STATE	ZIP CODE	COUNTRY
Yonezawa; Minoru	Tokyo			JP

US-CL-CURRENT: 369/44.34; 369/30.15, 369/44.25, 369/44.32

Full | Title | Citation | Front | Review | Classification | Date | Reference | Claims | KWMC | Draw De

☐ 5. Document ID: US 5974247 A

L2: Entry 5 of 6 File: USPT Oct 26, 1999

US-PAT-NO: 5974247
DOCUMENT-IDENTIFIER: US 5974247 A

TITLE: Apparatus and method of LSI timing degradation simulation

DATE-ISSUED: October 26, 1999

INVENTOR-INFORMATION:

NAME	CITY	STATE	ZIP CODE	COUNTRY
Yonezawa; Hirokazu	Hyogo			JP

US-CL-CURRENT: 703/19; 703/20, 716/6

Full | Title | Citation | Front | Review | Classification | Date | Reference | [illegible] | Claims | KWIC | Draw De

☐ 6. Document ID: US 5661413 A

L2: Entry 6 of 6 File: USPT Aug 26, 1997

US-PAT-NO: 5661413
DOCUMENT-IDENTIFIER: US 5661413 A

TITLE: Processor utilizing a low voltage data circuit and a high voltage controller

DATE-ISSUED: August 26, 1997

INVENTOR-INFORMATION:

NAME	CITY	STATE	ZIP CODE	COUNTRY
Tomita; Yasuhiro	Hyogo			JP
Shono; Toshiyuki	Kyoto			JP
Yonezawa; Hirokazu	Hyogo			JP

US-CL-CURRENT: 326/80

Full | Title | Citation | Front | Review | Classification | Date | Reference | [illegible] | Claims | KWIC | Draw De

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Term	Documents
SIMULATION	69847
SIMULATIONS	22322
TIMING	392383
TIMINGS	30936
(1 AND SIMULATION AND TIMING).PGPB,USPT.	6
(L1 AND SIMULATION AND TIMING).PGPB,USPT.	6